

Fig. 1(A)

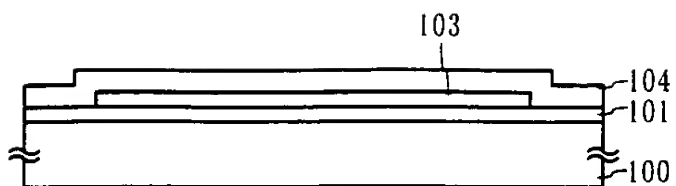


Fig. 1(B)

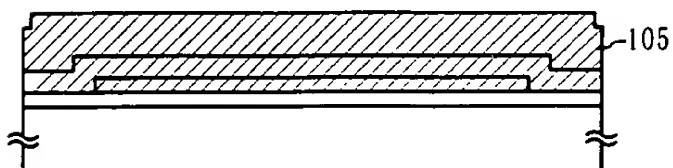


Fig. 1(C)

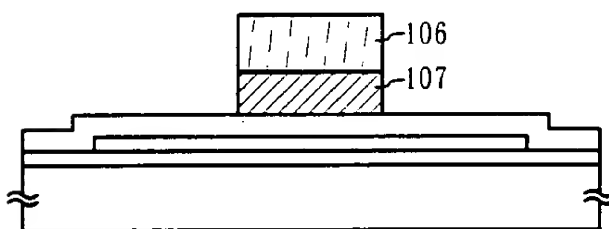


Fig. 1(D)

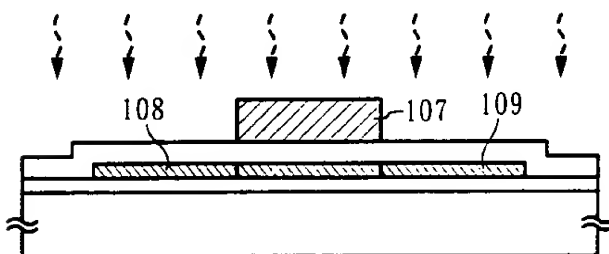


Fig. 2(A)

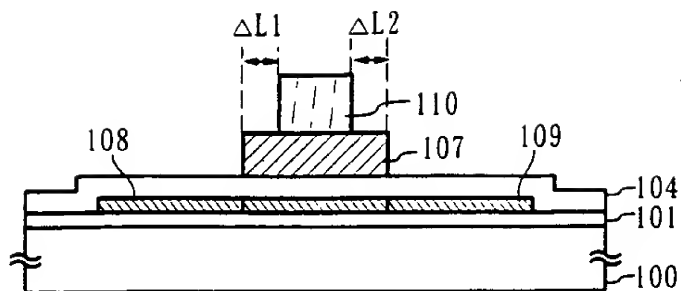


Fig. 2(B)

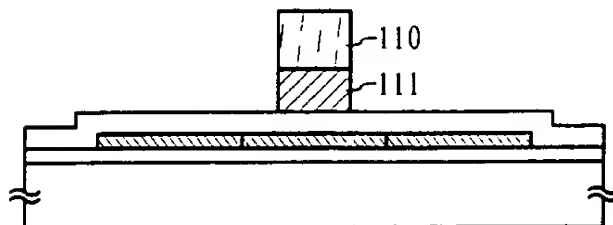


Fig. 2(C)

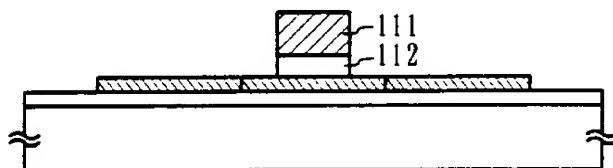


Fig. 2(D)

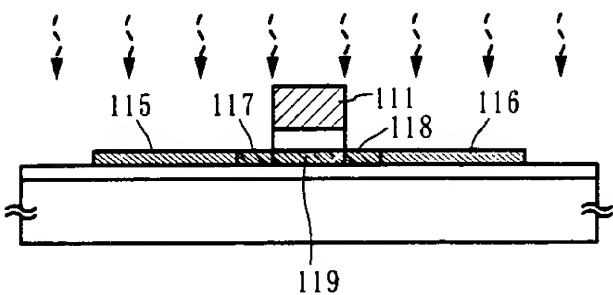
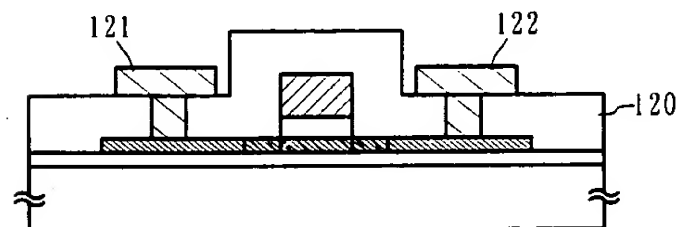


Fig. 2(E)



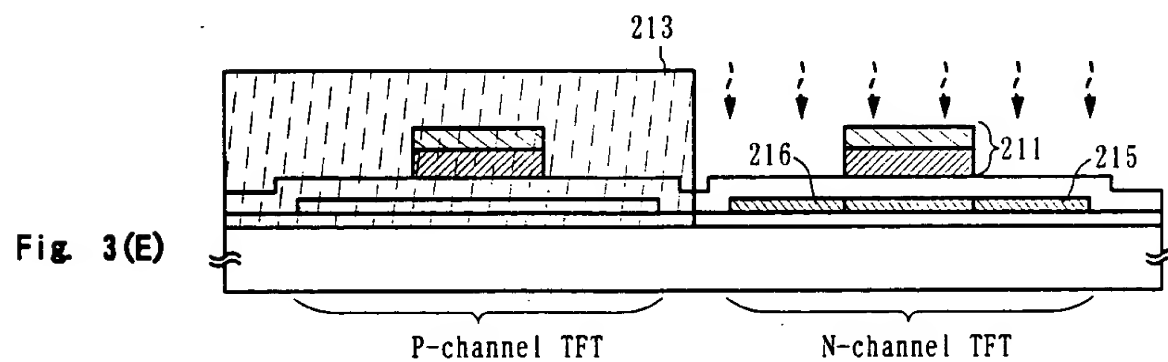
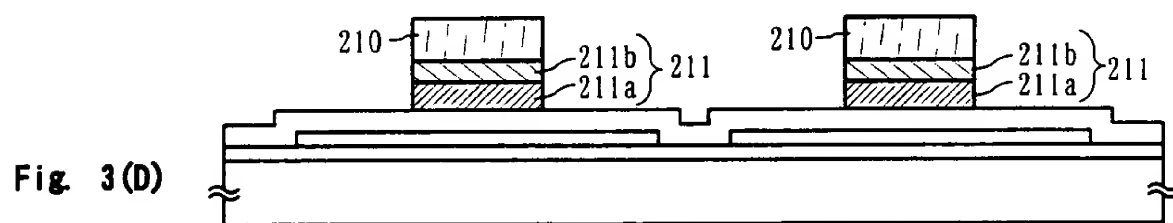
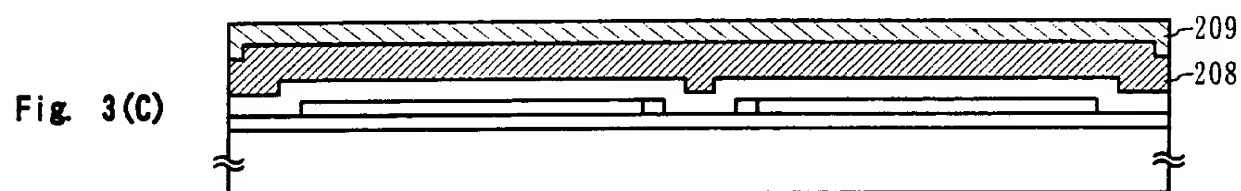
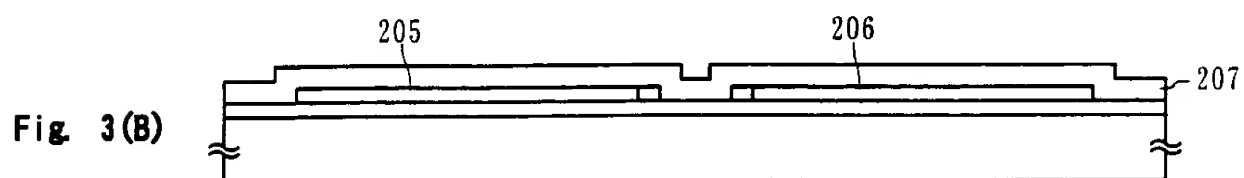
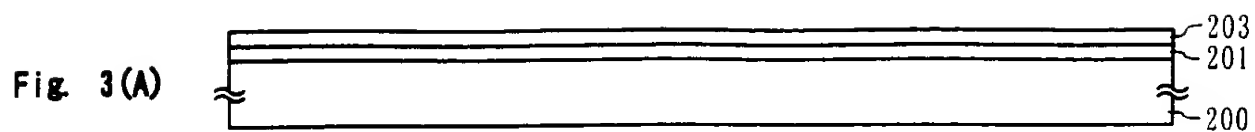


Fig 4(A)

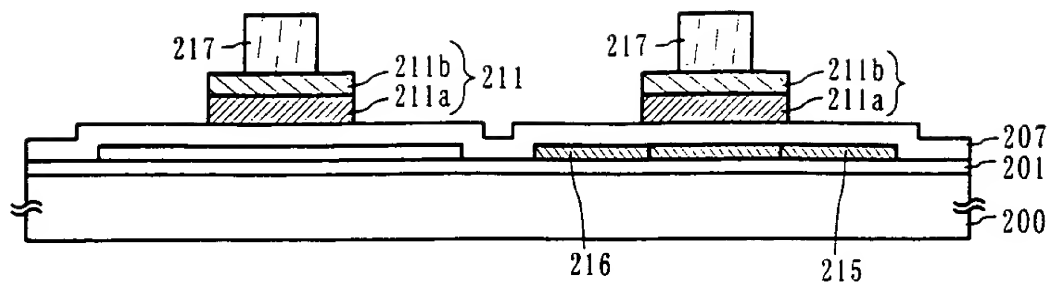


Fig 4(B)

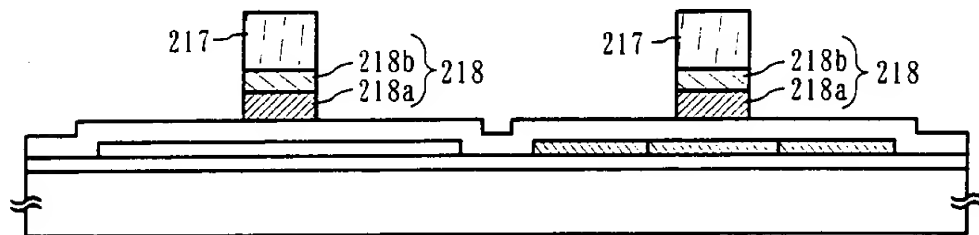


Fig 4(C)

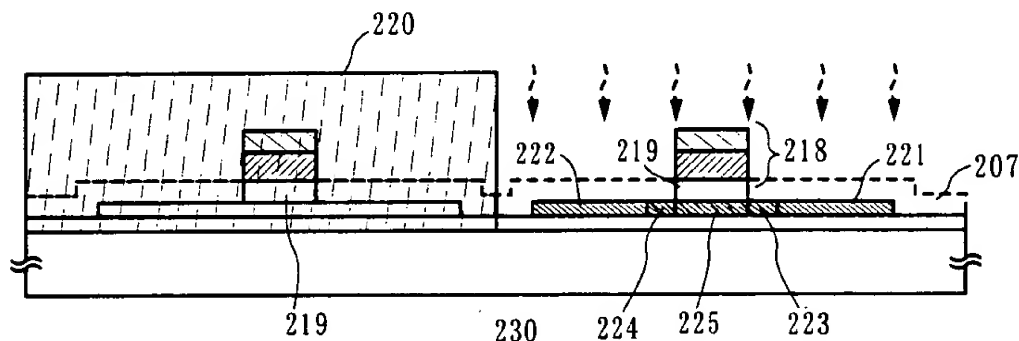


Fig 4(D)

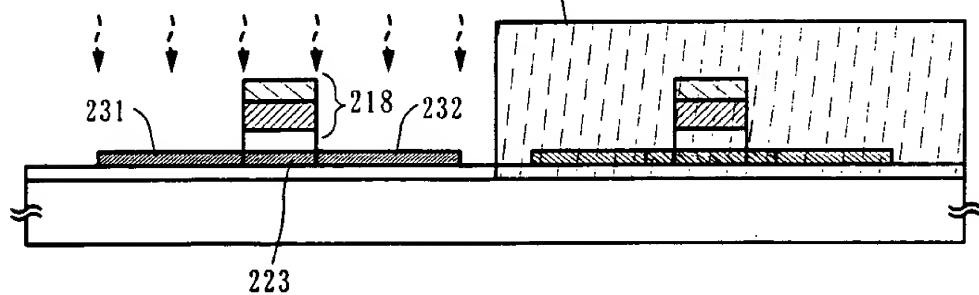
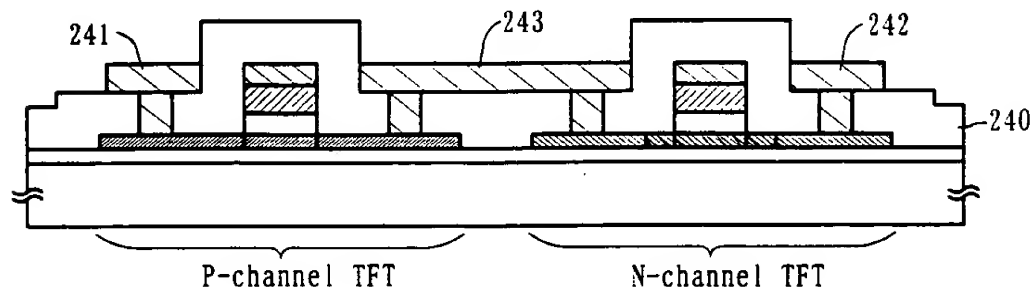


Fig 4(E)



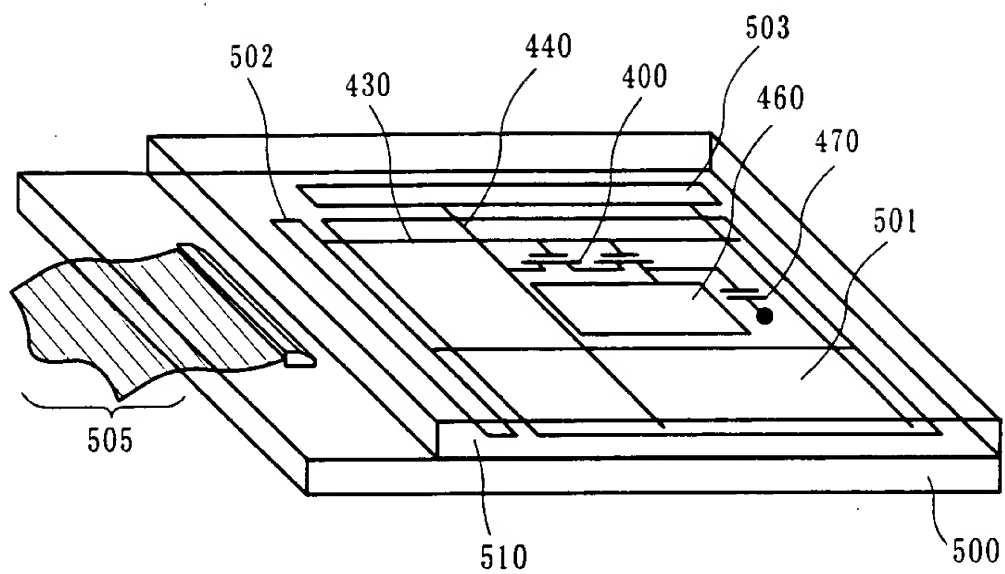


Fig. 5

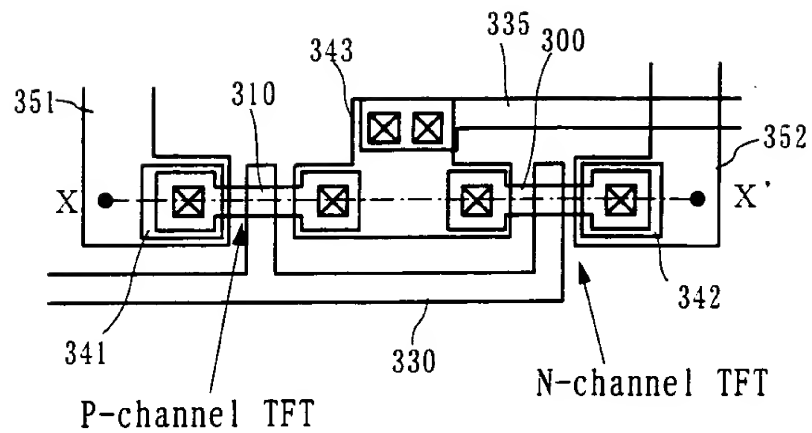


Fig. 6(A) Top View of a CMOS Circuit

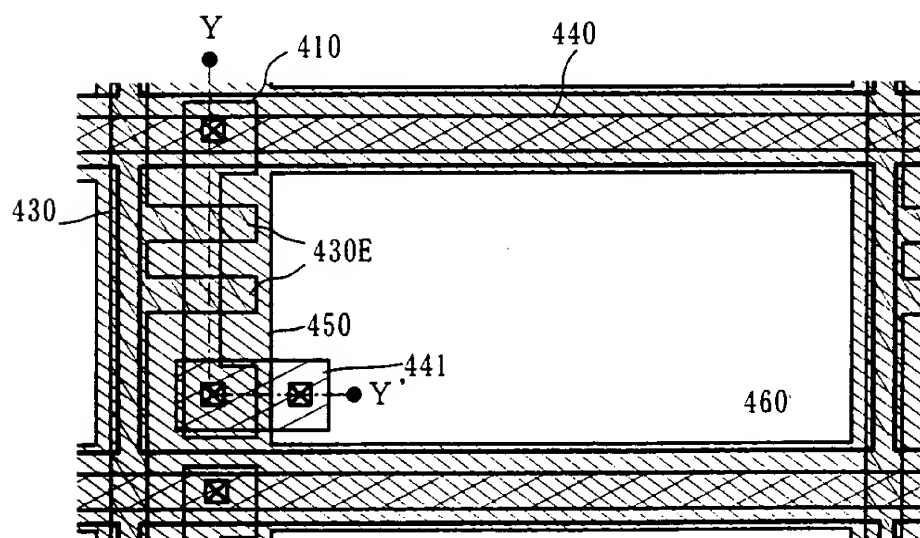


Fig. 6(B) Top View of a Pixel Matrix Circuit 301

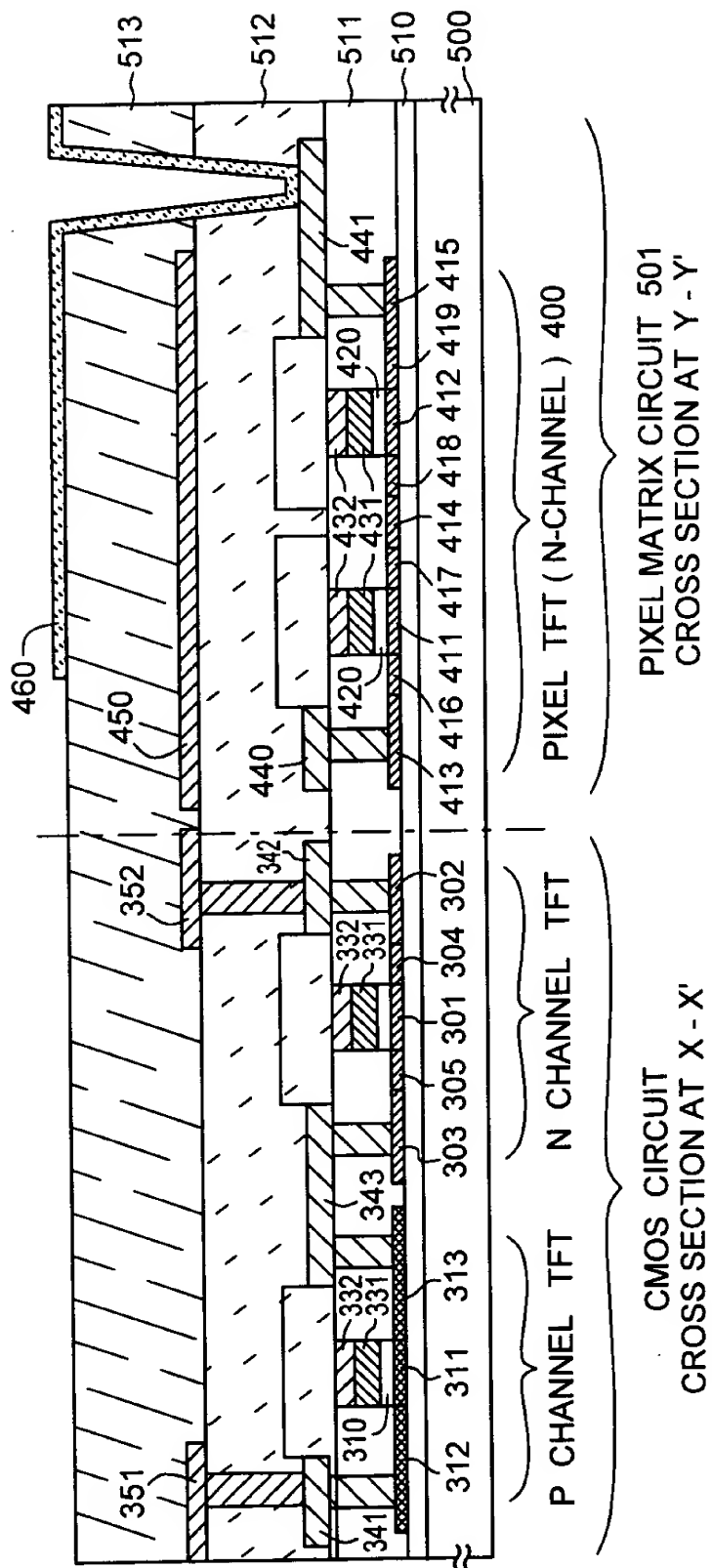


FIG. 7

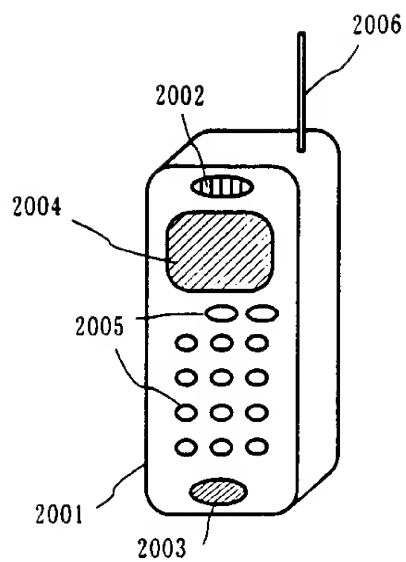


Fig. 8(A)

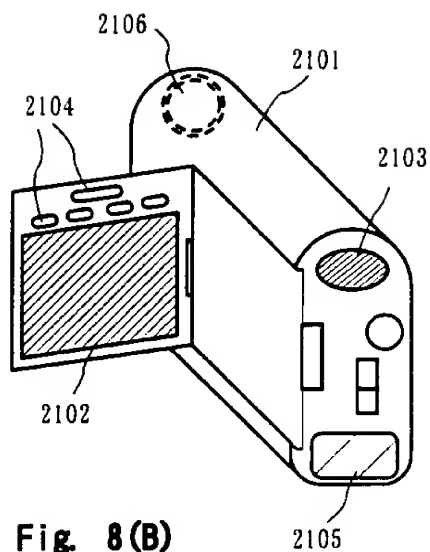


Fig. 8(B)

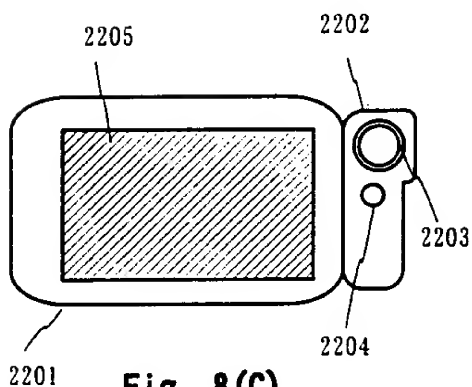


Fig. 8(C)

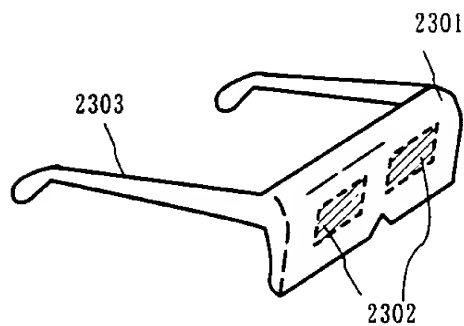


Fig. 8(D)

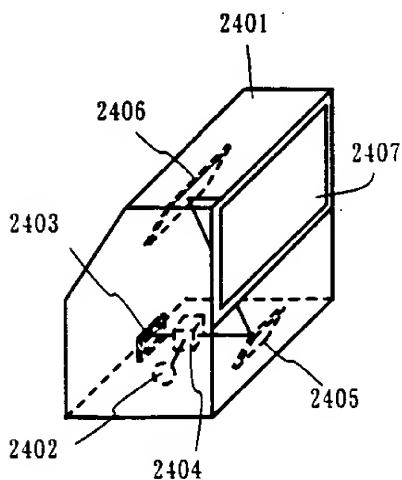


Fig. 8(E)

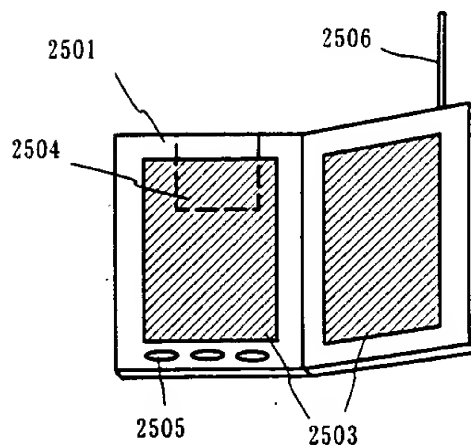


Fig. 8(F)

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Fig. 9(A)
Prior Art

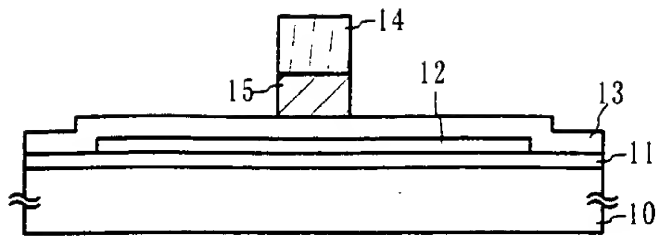


Fig. 9(B)
Prior Art

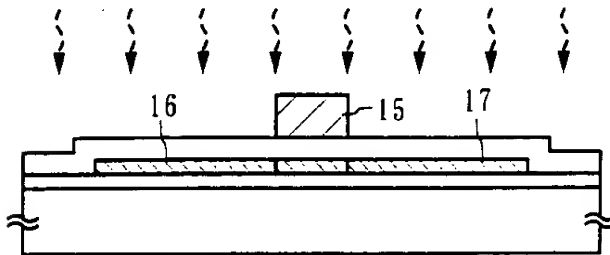


Fig. 9(C)
Prior Art

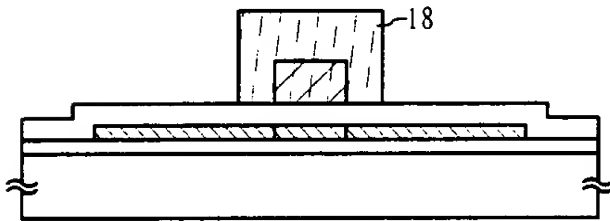


Fig. 9(D)
Prior Art

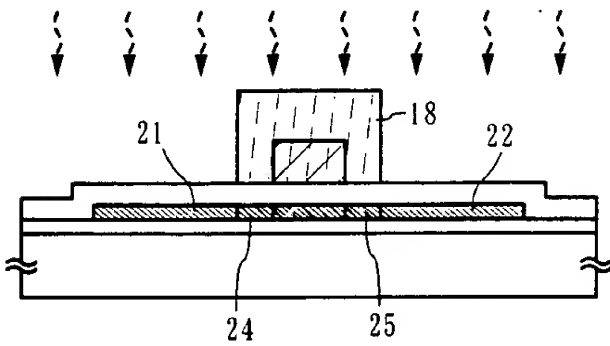
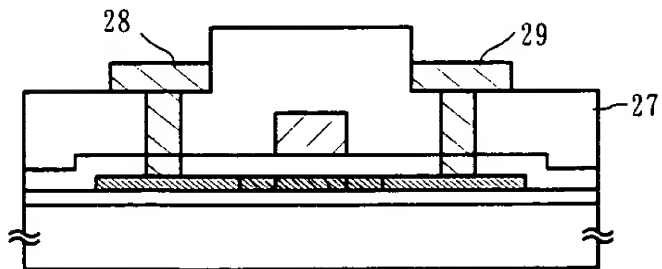


Fig. 9(E)
Prior Art



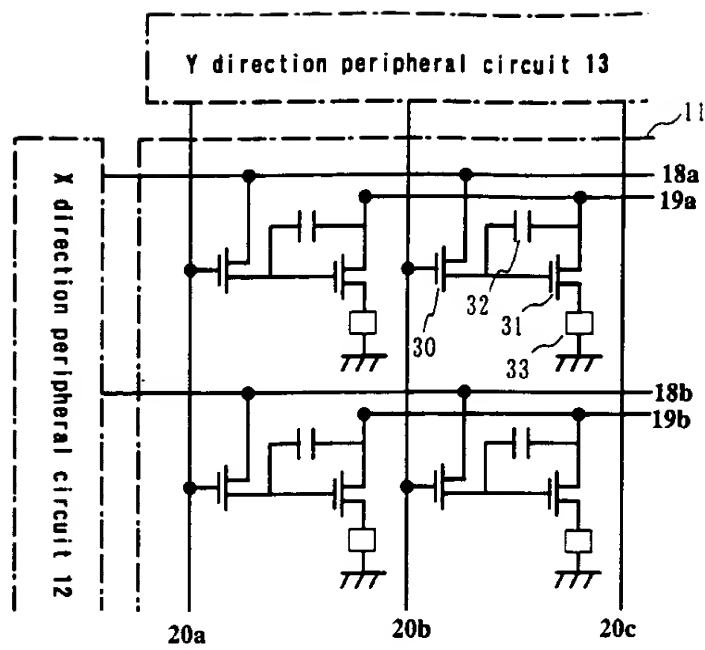


Fig. 10(A) EL Panel Circuit Diagram

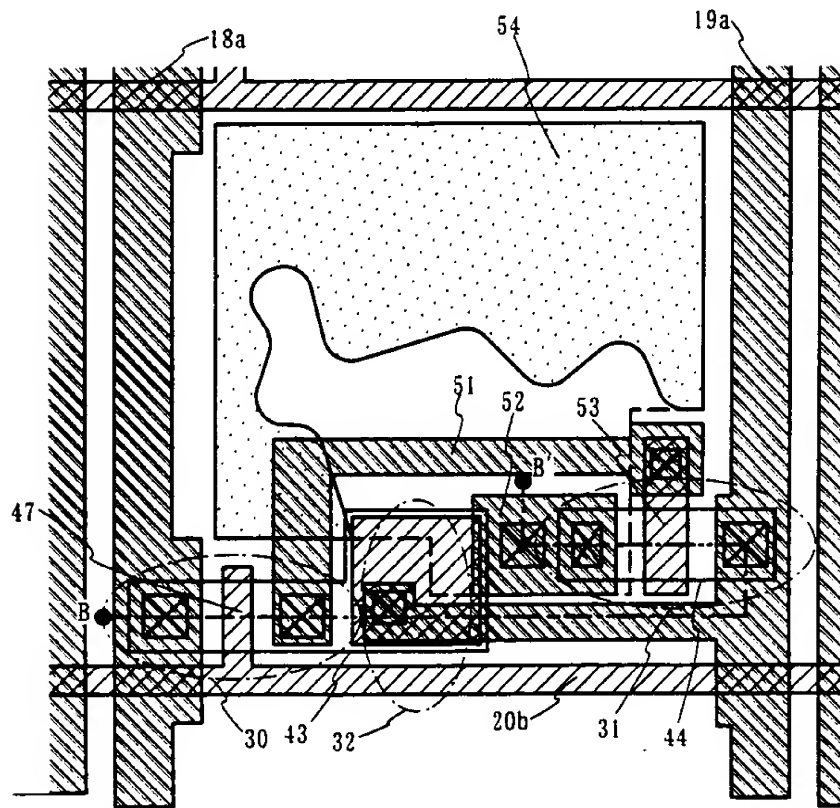


Fig. 10(B) Top View of EL Panel Pixel

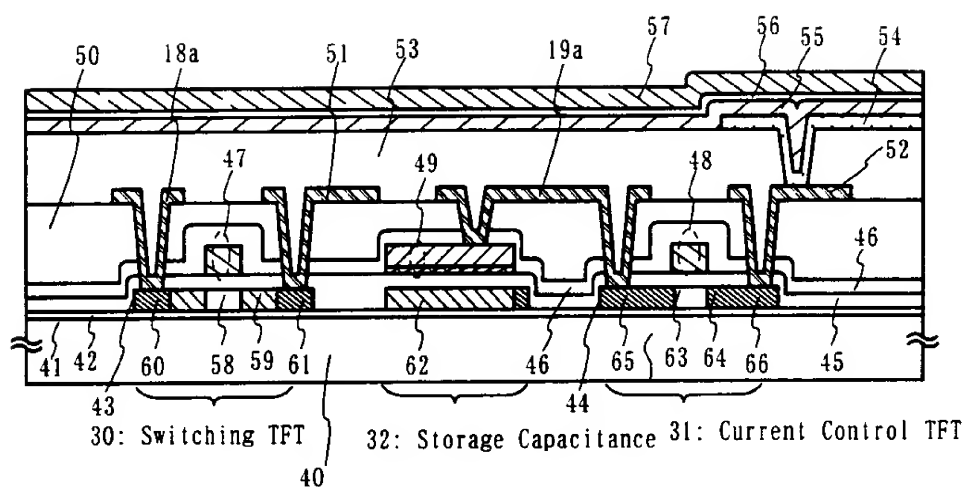


Fig. 11

FIG. 12A

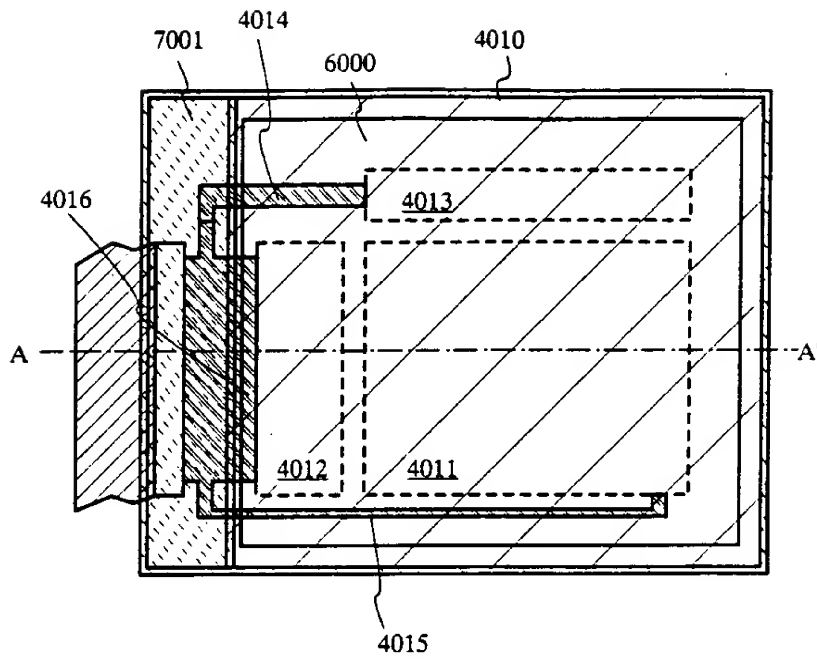


Fig. 12A

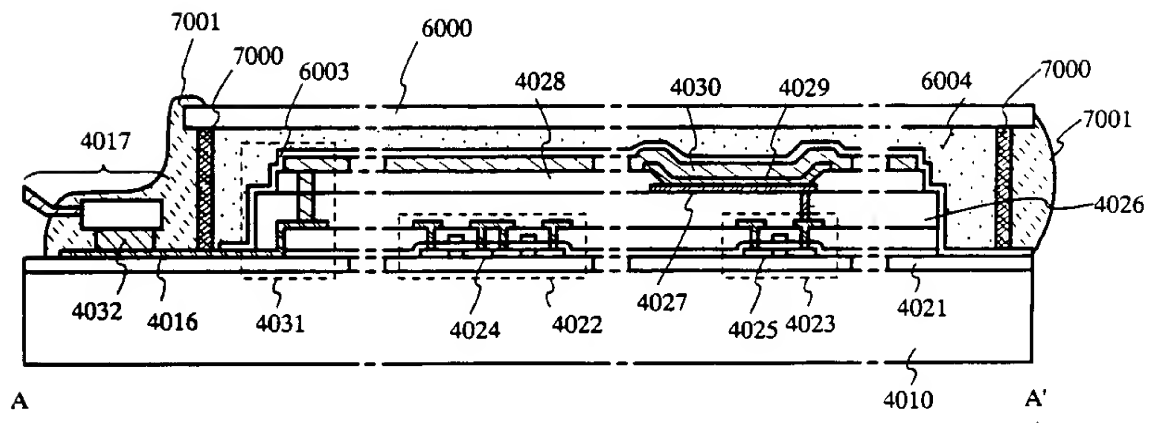
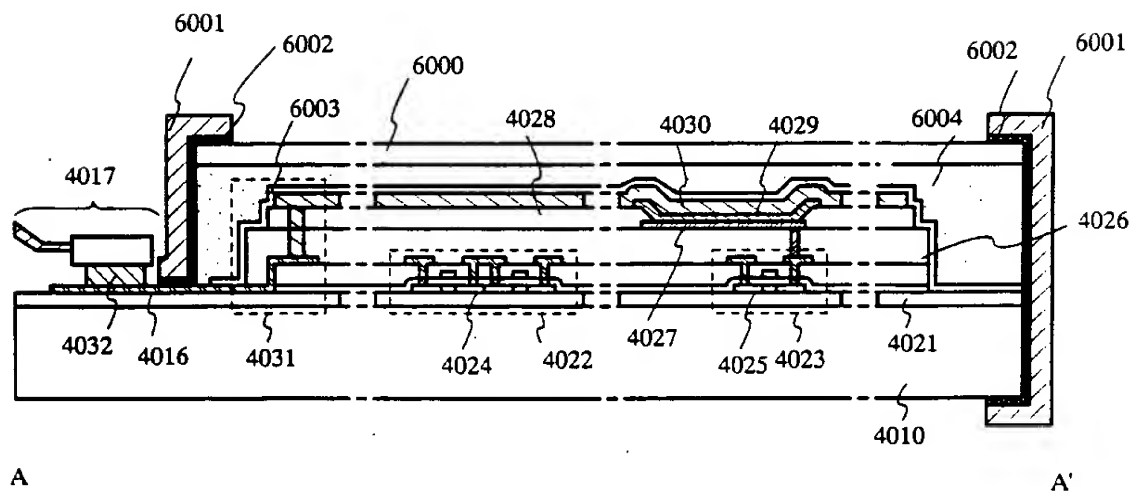
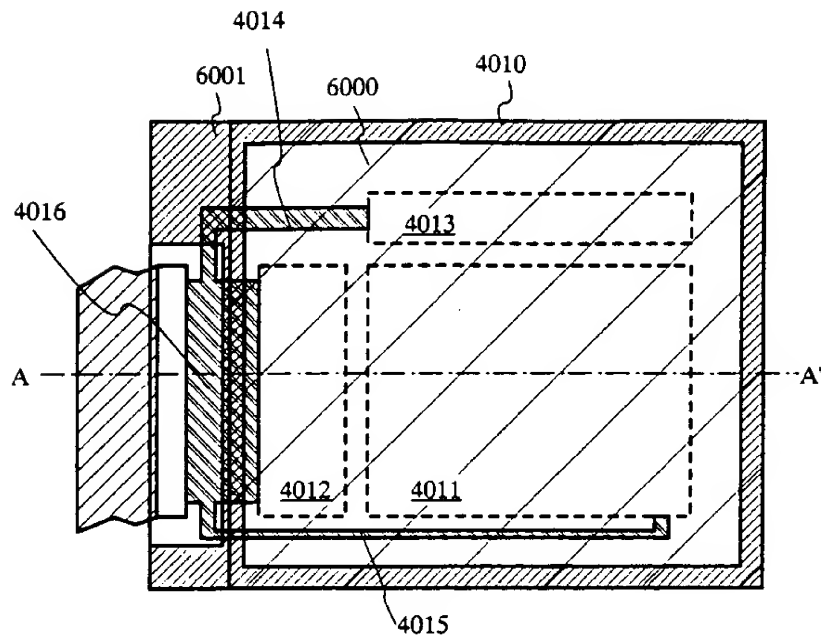


Fig. 12B



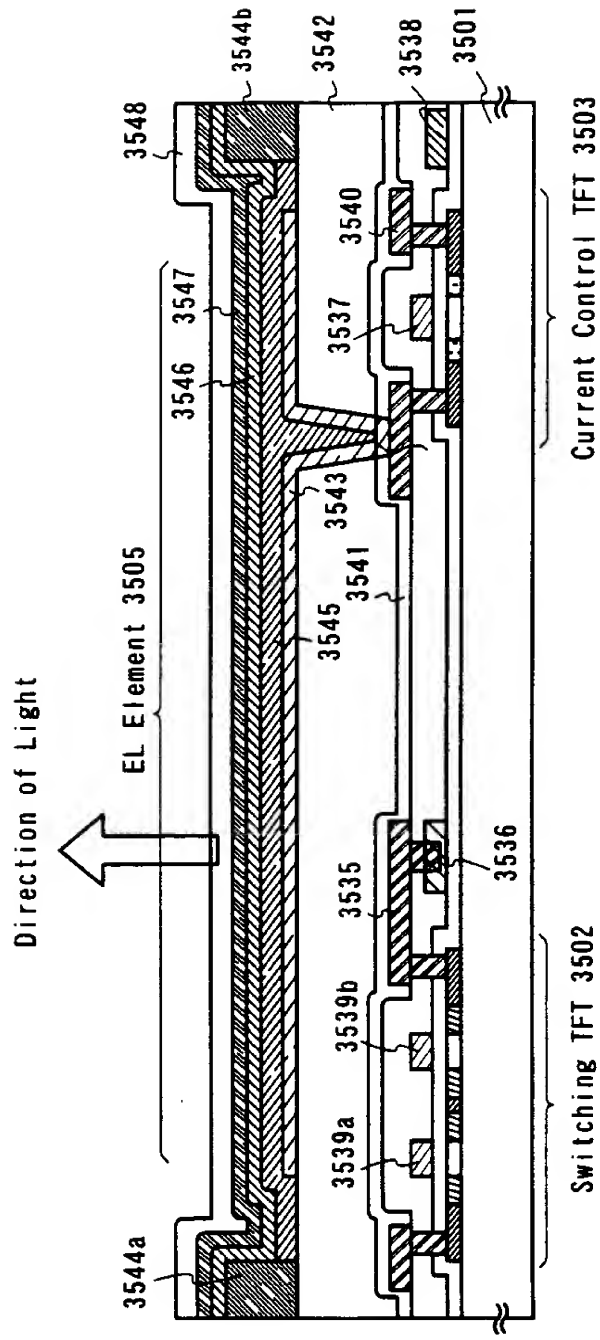
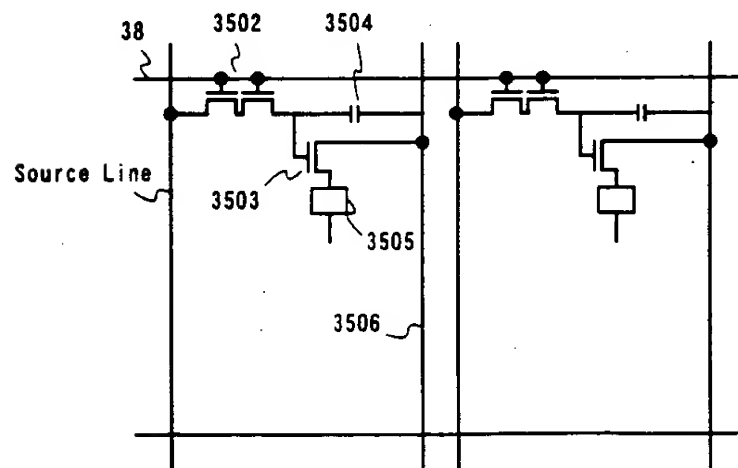
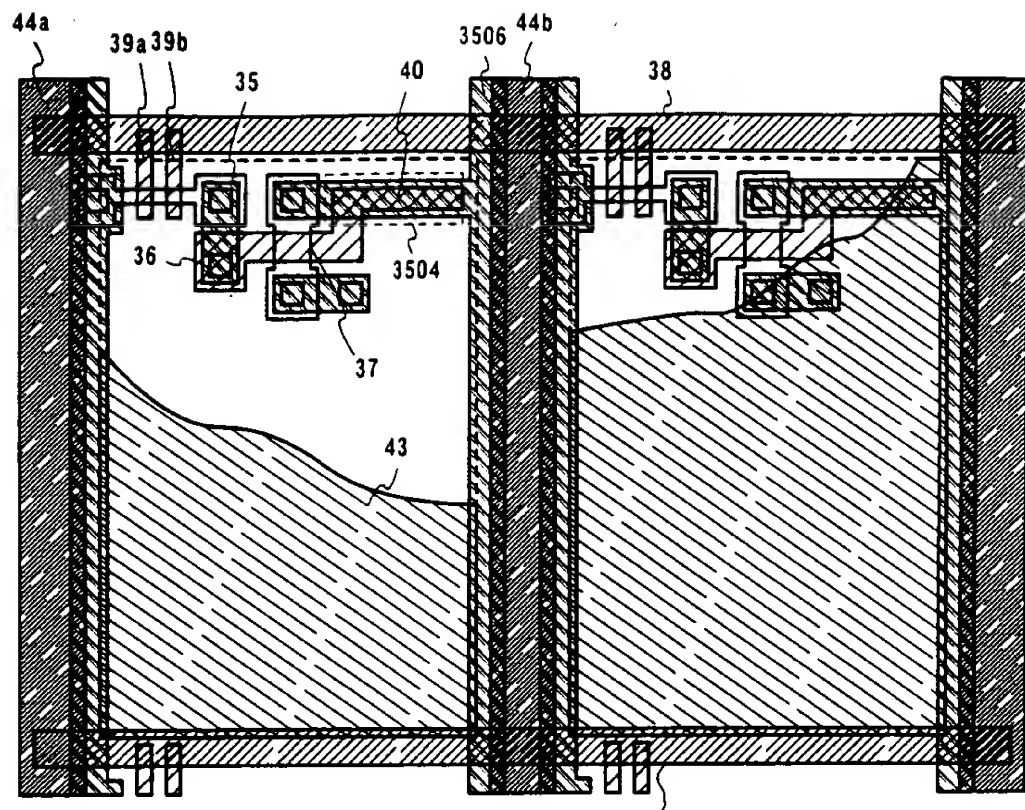


Fig. 14



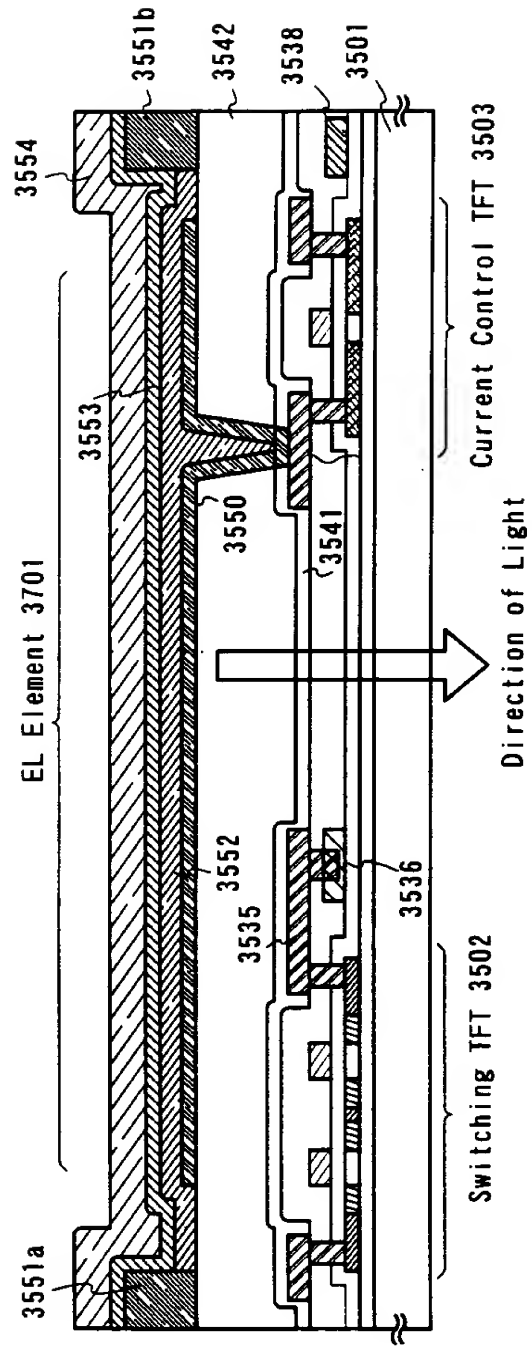


Fig. 16

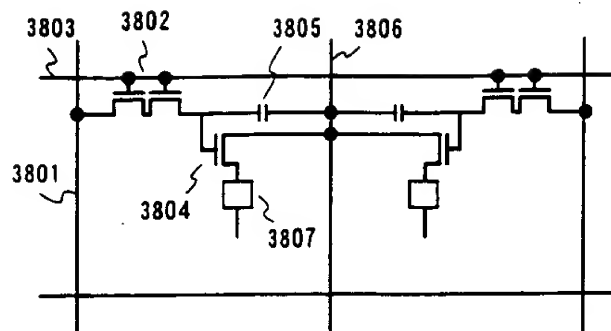


Fig. 17A

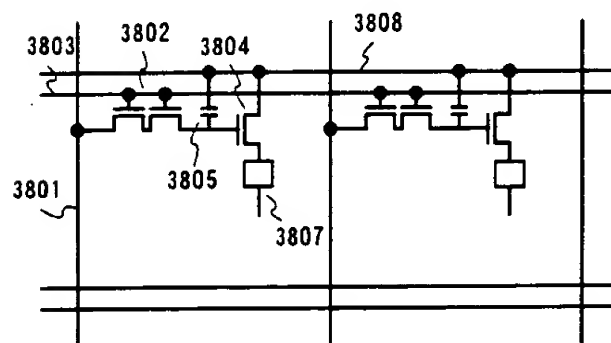


Fig. 17B

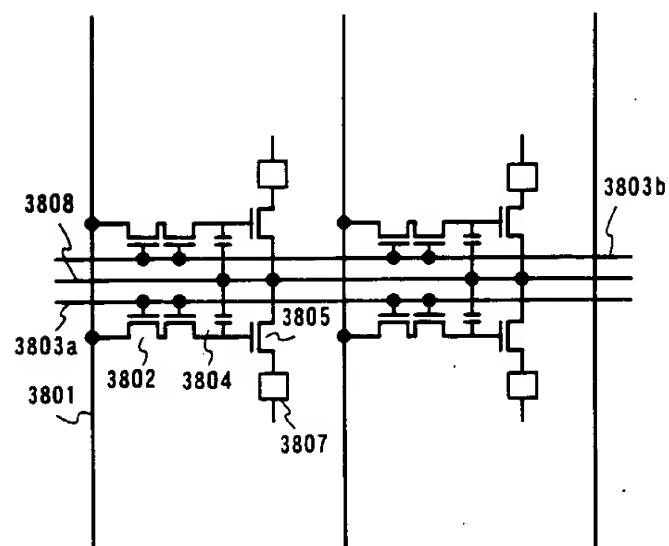


Fig. 17C